Two-Wire Serial EEPROM
64K (8-bit wide)

FEATURES

- Low voltage and low power operations:
  - FT24C64C: V_{CC} = 1.7V to 5.5V
- Maximum Standby current < 1μA (typically 0.02μA and 0.06μA @ 1.7V and 5.5V respectively).
- 32 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 8,192 × 8 (64K).
- Addition identification page.
- Configurable device address.
- Programmable Software Write protect:
  - Upper quarter memory array
  - Upper half memory array
  - Upper 3/4 memory array
  - Whole memory array
- Standard 2-wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed Write Cycle (5ms maximum).
- 1000 kHz (2.5V~5V), 400 kHz (1.7V) Compatibility.
- Automatic erase before write operation.
- High reliability: typically 1,000,000 cycles endurance.
- 100 years data retention.
- Industrial temperature range (-40℃ to 85℃).
- Standard CSP Pb-free package.

DESCRIPTION

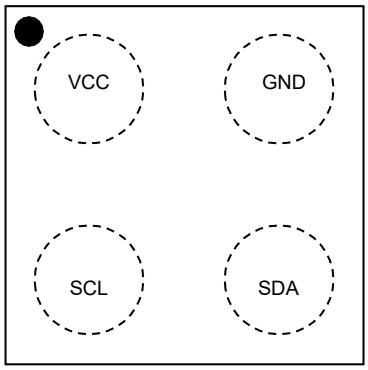
The FT24C64C series are 65,536 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 8,192 words of 8 bits (one byte) each. They offer an additional page (Identification Page) of 32 bytes. They also provide the Write Device Address instruction for users to implement configurable device address features. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. The device features programmable software write protection which provides partial as well as full memory array protection. These devices are available in thin 4-ball WLCSP package. A standard 2-wire serial interface is used to address all read and write functions. Our extended VCC range (1.7V to 5.5V) devices enable wide spectrum of applications.

PIN CONFIGURATION

Pin Name	Pin Function
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
VCC	Power Supply
GND	Ground

All these packaging types come in Pb-free certified.

FT24C64C



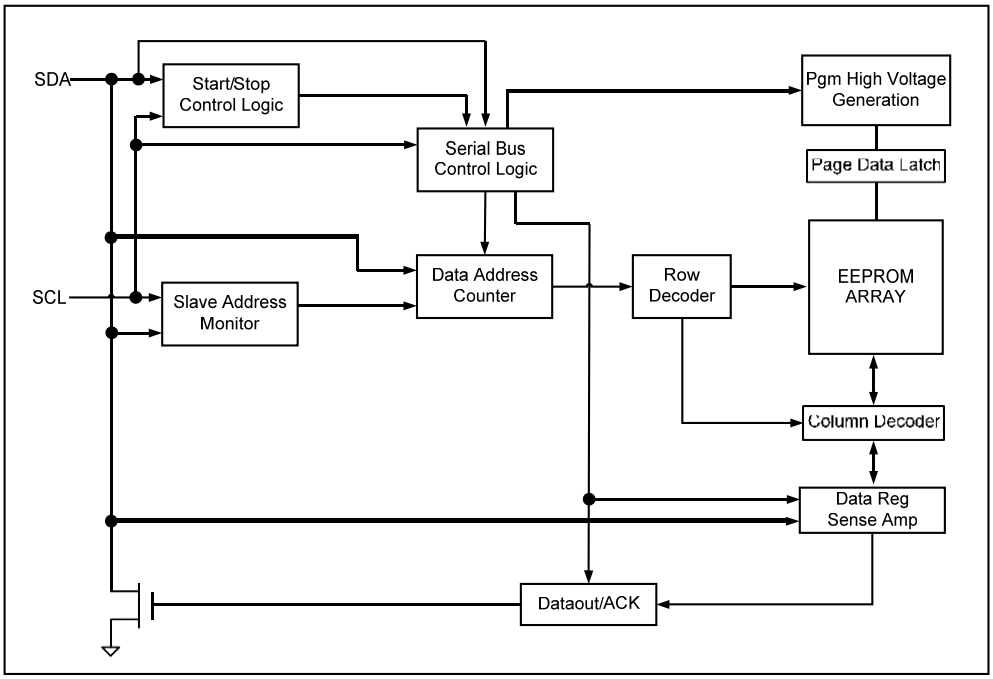
Thin 4-ball WLCSP
(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40℃ to 85℃
Storage temperature:	-50℃ to 125℃
Input voltage on any pin relative to ground:	-0.3V to V_{CC} +0.3V
Maximum voltage:	8V
ESD Protection on all pins:	HBM >6000V

** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality*.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

MEMORY ORGANIZATION

The FT24C64C devices have 256 pages and an Identification page respectively. Since each page has 32 bytes, random word addressing to FT24C64C will require 13 bits data word addresses respectively.

DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at V_{IL}. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL ≥ V_{IH}, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL ≥ V_{IH}, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish (see Figure 1).

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9th serial clock after each word.

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

(F) SOFT RESET

After an interruption in protocol power loss or system reset, any two-wire part can be reset by following these steps:

1. Create a START condition,
2. Clock eighteen data bits “1”,
3. Create a START condition as SDA is high.

Figure 1: Timing diagram for START and STOP conditions

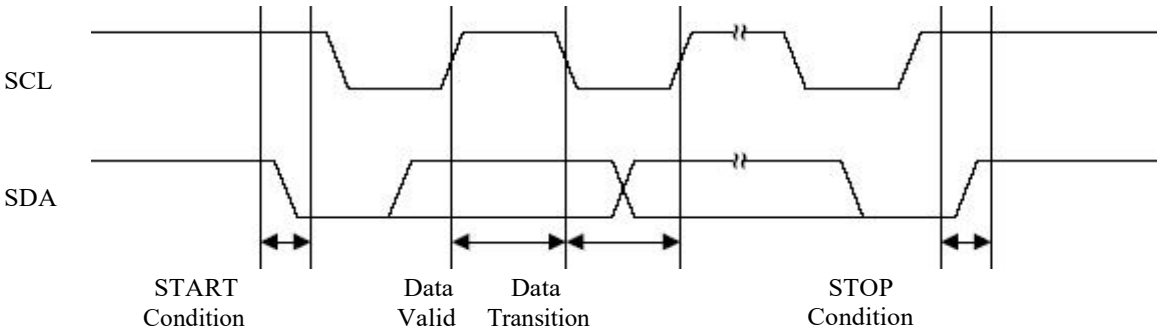
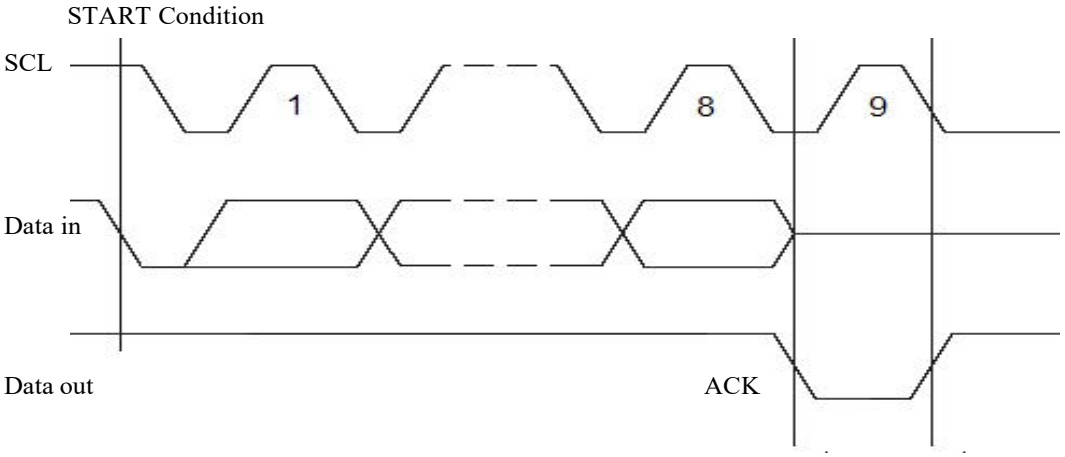


Figure 2: Timing diagram for output ACKNOWLEDGE



DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke a valid read or write command. The first four most significant bits of the device address should be 1010 or 1011, the next three bits are device address bits. These three device address bits (5th, 6th and 7th) are to match with the configurable device address E2/E1/E0. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8th read/write bit, otherwise the chip will go into STANDBY mode. Since there are no A2/A1/A0 pins, FT24C64C provides the Write Device Address instruction for users to implement configurable device address features. When power-on, the device will load the configured device address E2/E1/E0 automatically. The device address factory default value is "000". The last or 8th bit is a read/write command bit. If the 8th bit is at V_{IH} then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

Table1-1. Device address

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal area	1	0	1	0	E2	E1	E0	R/W
SWP(1)	1	0	1	0	E2	E1	E0	R/W
WDA(2)	1	0	1	1	E2	E1	E0	0

Table1-2. Word address0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal area	0	x	x	A12	A11	A10	A9	A8
SWP	1	x	x	x	x	x	x	x
WDA	x	x	x	x	x	0	1	x

Table1-3. Word address1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal area	A7	A6	A5	A4	A3	A2	A1	A0
SWP	x	x	x	x	x	x	x	x
WDA	x	x	x	x	x	x	x	x

Notes: (1) SWP is short for Software Write Protection;

(2) WDA is short for Write Device Address.

X = Don't care bit.

WRITE OPERATIONS

(A) BYTE WRITE

A write operation requires two 8-bit data word address following the device address word and ACKNOWLEDGE signal. Upon receipt of this address, the EEPROM will respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will again output a "0". The addressing device, such as a microcontroller, must terminate the write sequence with a STOP condition. At this time the EEPROM enters into an internally-timed write cycle state. All inputs are disabled during this write cycle and the EEPROM will not respond until the writing is completed (figure 3).

(B) PAGE WRITE

The 64K EEPROM are capable of 32-byte page write.

A page write is initiated the same way as a byte write, but the microcontroller does not send a STOP condition after the first data word is clocked in. The microcontroller can transmit up to 31 more data words after the EEPROM acknowledges receipt of the first data word. The EEPROM will respond with a

"0" after each data word is received. The microcontroller must terminate the page write sequence with a STOP condition (see Figure 4).

The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than 32 data words are transmitted to the EEPROM, the data word address will "roll over" and the previous data will be overwritten.

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

(D) WRITE IDENTIFICATION PAGE

The Identification Page (32 bytes) is an additional page. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write, except for the following differences:

Device type identifier = 1011;

MSB address bits A15-A5 are don't care except for address bits A10/A9 which must be equal to "00". LSB address bits A4-A0 define the byte address inside the Identification page.

(E) WRITE DEVICE ADDRESS

The configurable device address can be written by issuing the Write Device Address instruction. This instruction uses the same protocol and format as Byte Write, except for the following differences:

Device type identifier = 1011;

Address bit A10/A9 must be "01", all other address bits are don't care;

The data byte must be equal to the binary value xxxx xE2E1E0, where x is don't care and E2E1E0 is the new device address.

(F) SOFTWARE WRITE PROTECTION

The user can select to write-protect partial or full memory array by writing a specific data into the Write Protect Register (WPR). The WPR is located outside of the 8K bytes memory addressing space, at address 1xxx.xxxx.xxxx.xxxxb.

The write protect control bits, b1 to b3 are non-volatile.

The WPEN (Write Protect Enable) bit enables the write protection when it is set to "1". When the WPEN bit is "0", the whole memory array can be written.

The BP0 and BP1 (Block Protect) bits determine which area is write protected. The user can select to protect a quarter, one half, three quarters or the entire memory by setting these bits according to Table3. The protected blocks then become read-only.

The FT24C64C will not acknowledge the data byte and the write request will be rejected for the addresses located in the protected area. Writing in the Write protect register is performed with a Byte Write instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7/b6/b5/b4/b0 of the data byte are not significant (Don't Care). Writing more than one byte will discard the write cycle (Write protect register content will not be changed).

Table2. Write Protect Register (WPR)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WRITE	X	X	X	X	WPEN	BP1	BP0	X
READ	0	0	0	0	WPEN	BP1	BP0	0

Table3: Block Protect

BP1	BP0	ARRAY ADDRESS PROTECTED	PROTECTION
0	0	1800 - 1FFF	Upper Quarter Protection
0	1	1000 - 1FFF	Upper Half Protection
1	0	0800 - 1FFF	Upper 3/4 Array Protection
1	1	0000 - 1FFF	Full Array Protection

READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to “1”. The read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8th) set to “1”. The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode (see Figure 5).

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8th) set to “1”. The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one.

Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead (figure 6).

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a “dummy write” instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to “0”. The EEPROM will then acknowledge. The micro-controller will then send two address words. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM

will reset the internal programming process and continue to execute the new instruction - which is to read the current address (figure 7).

(D) READ IDENTIFICATION PAGE

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as the Random Read with device type identifier defined as “1011”. The MSB address bits A15-A5 are don’t care, the LSB address bits A4-A0 define the byte address inside the Identification Page.

(E) READ WPR

Reading the write protect register is performed with a Random Read instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7/b6/b5/b4/b0 of the write protect register content are read as 00000. The signification of the protect register lower bits b3/b2/b1 are defined previously.

Reading more than one byte will loop on reading the configuration register value. The configuration register cannot be read while a write cycle is ongoing.

Figure 3: Byte Write

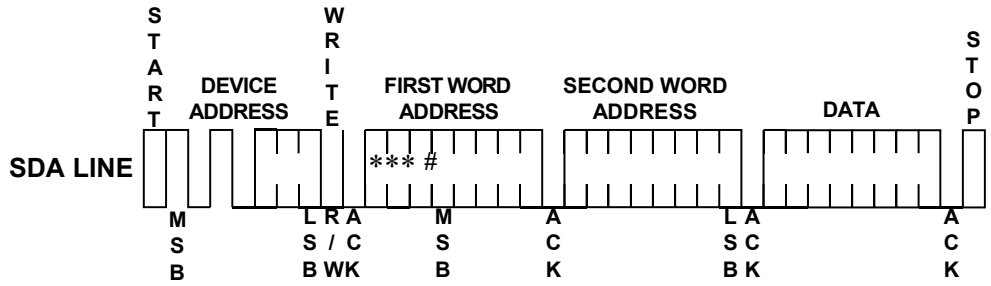


Figure 4: Page Write

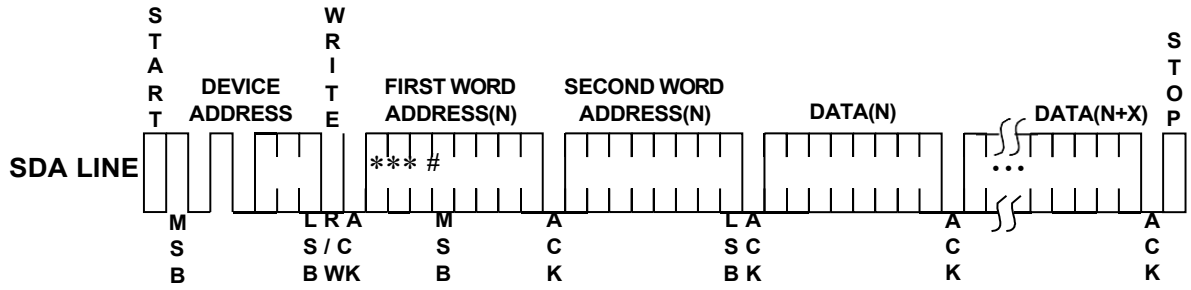


Figure 5: Current Address Read

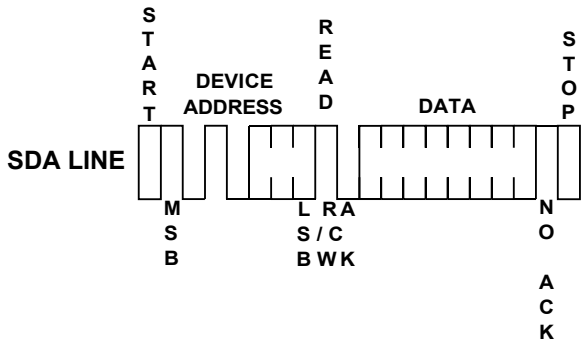


Figure 6: Sequential Read

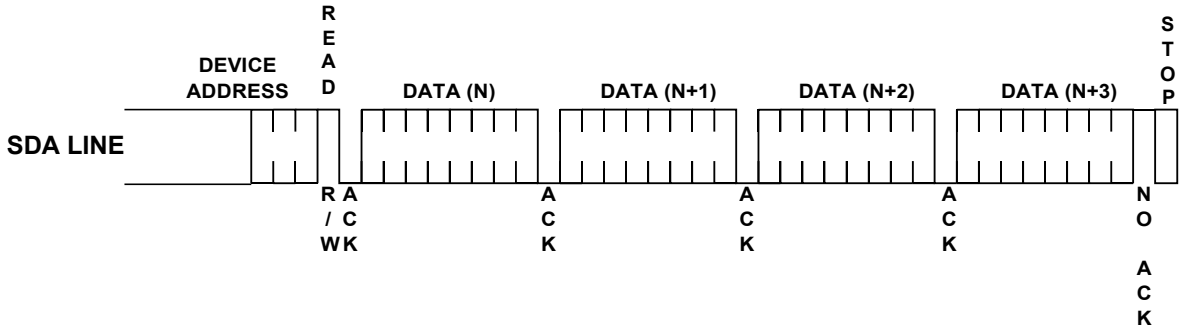
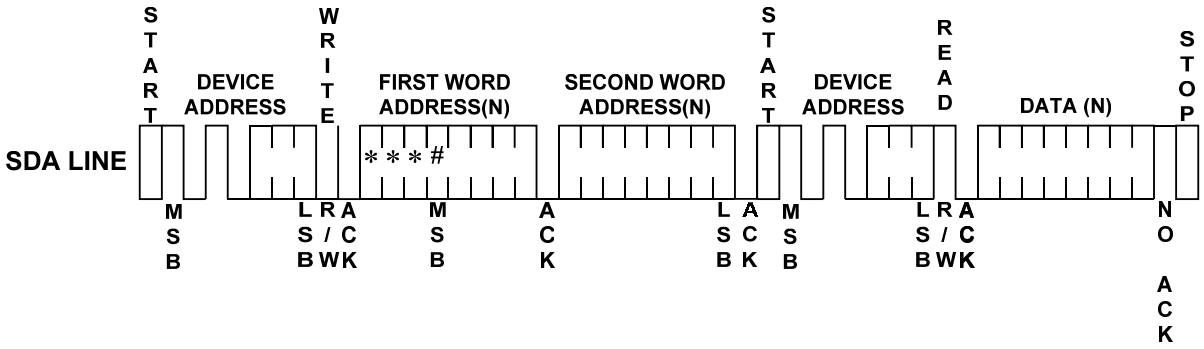
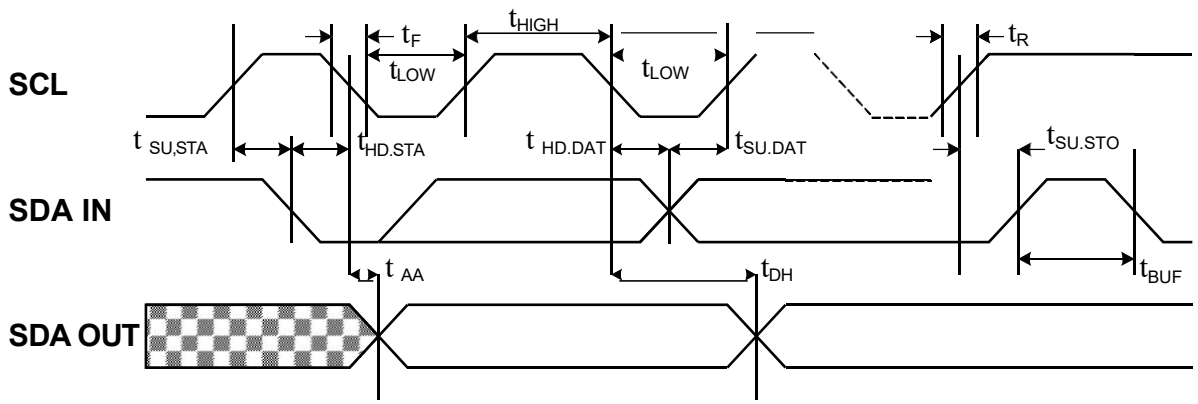


Figure 7: Random Read



Notes: 1) * = Don’t Care bits

Figure 8: SCL and SDA Bus Timing



Electrical Specifications

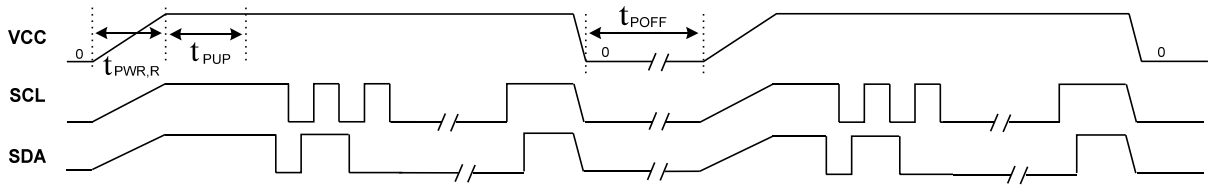
(A) Power-Up Requirements

During a power-up sequence, the VCC supplied to the device should monotonically rise from GND to the minimum VCC level, with a slew rate no faster than 0.05 V/μs and no slower then 0.1 V/ms. A decoupling cap should be connected to the VCC PAD which is no smaller than 10nF.

(B) Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, this device includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the VCC level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode. The system designer must ensure the instructions are not sent to the device until the VCC supply has reached a stable value greater than or equal to the minimum VCC level.

Figure 9: Power on and Power down



If an event occurs in the system where the VCC level supplied to the device drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the VCC pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

AC CHARACTERISTICS

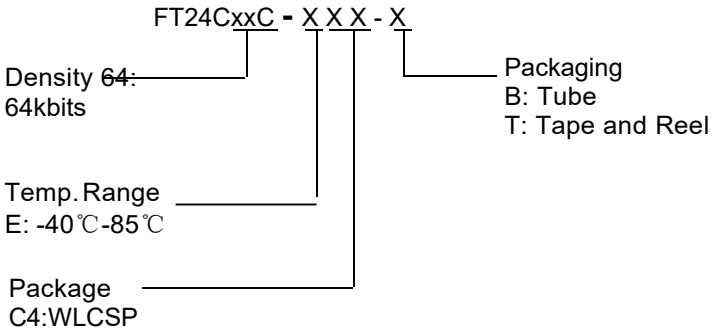
Symbol	Parameter	1.7V		2.5-5.5 V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL		400		1000	kHz
t_{LOW}	Clock pulse width low	1.2		0.6		μs
t_{HIGH}	Clock pulse width high	0.4		0.3		μs
t_I	Noise suppression time(1)		80		40	ns
t_{AA}	Clock low to data out valid	0.3	1.2	0.2	0.5	μs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		1.2		μs
$t_{HD.STA}$	START hold time	0.6		0.6		μs
$t_{SU.STA}$	START set-up time	0.6		0.6		μs
$t_{HD.DAT}$	Data in hold time	50		50		ns
$t_{SU.DAT}$	Data in set-up time	100		100		ns
t_R	Input rise time(1)		300		300	ns
t_F	Input fall time(1)		300		300	ns
$t_{SU.STO}$	STOP set-up time	0.6		0.6		μs
t_{DH}	Date out hold time	200		200		ns
$t_{PWR,R}$	Vcc slew rate at power up	0.1	50	0.1	50	V/ms
t_{PUP}	Time required after VCC is stable before the device can accept commands	100		100		μs
t_{POFF}	Minimum time at Vcc=0V between power cycles	500		500		ms
t_{WR}	Write cycle time		5		5	ms
Endurance(1)	25ºC, Page Mode, 3.3V	1,000,000				Write Cycles

Notes:
1. This Parameter is expected by characterization but are not fully screened by test.
2. AC Measurement conditions:
   RL (Connects to Vcc): 1.3KΩ
   Input Pulse Voltages: 0.3Vcc to 0.7Vcc
   Input and output timing reference Voltages: 0.5Vcc

DC CHARACTERISTICS

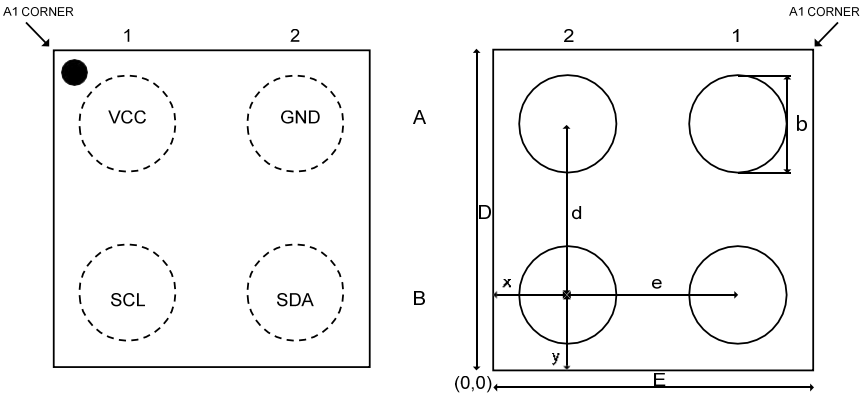
Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
V_{CC1}	24C××A supply V_{CC}		1.7		5.5	V
I_{CC}	Supply read current	V_{CC} @ 5.5V SCL = 400 kHz		0.4	1.0	mA
I_{CC}	Supply write current	V_{CC} @ 5.5V SCL = 400 kHz		2.0	3.0	mA
I_{SB1}	Supply current	V_{CC} @ 1.7V, V_{IN} = V_{CC} or V_{SS}			1.0	μA
I_{SB2}	Supply current	V_{CC} @ 2.5V, V_{IN} = V_{CC} or V_{SS}			1.0	μA
I_{SB3}	Supply current	V_{CC} @ 5.5V, V_{IN} = V_{CC} or V_{SS}			1.0	μA
I_{IL}	Input leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	μA
I_{LO}	Output leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	μA
V_{IL}	Input low level		-0.6		V_{CC}× 0.3	V
V_{IH}	Input high level		V_{CC}× 0.7		V_{CC} + 0.5	V
V_{OL2}	Output low level	V_{CC} @ 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output low level	V_{CC} @ 1.7V, I_{OL} = 0.15 mA			0.2	V

ORDERING INFORMATION

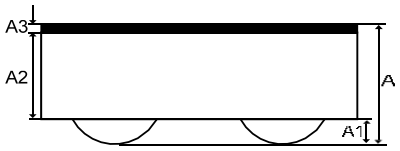


Density	Package	Temperature Range	Vcc	HSF	Packaging	Ordering Code
64kbits	WLCSP	-40℃-85℃	1.7V-5.5V	Green	Tape and Reel	FT24C64C-EC4-T

WLCSP PACKAGE OUTLINE DIMENSIONS



TOP VIEW BALL VIEW



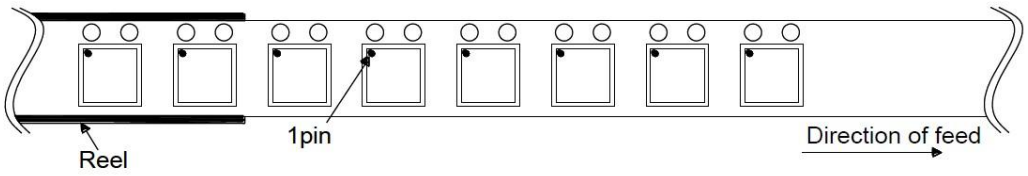
SIDE VIEW

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	TYP	Max	Min	TYP	Max
A	0.260	0.280	0.300	0.0102	0.0110	0.0118
A1	0.047	0.055	0.063	0.0019	0.0022	0.0025
A2	0.200REF			0.0079REF		
A3	0.020	0.025	0.030	0.0008	0.0010	0.0012
b	0.160	0.180	0.200	0.0063	0.0071	0.0079
D	0.666	0.691	0.716	0.0262	0.0272	0.0282
E	0.630	0.655	0.680	0.0248	0.0258	0.0268
d	-	0.400	-	-	0.0157	-
e	-	0.400	-	-	0.0157	-
x	0.115	0.128	0.140	0.0045	0.0050	0.0055
y	0.133	0.146	0.158	0.0052	0.0057	0.0062

Note:
1. Controlled dimensions are in millimeters
2. Drawing is not in scale

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



REVISION HISTORY

Revision	Date	Descriptions
B2	Feb.2020	Initial version.
B3	Apr. 2020	Added tape and reel information.

联系信息

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